1. Vidiot Deluxe Self-Test

The Vidiot Deluxe module has as part of integrated circuit U9, a program designed to test the module each time power is applied. No action is required on the operator's part to initiate the test. The program causes the MPU chip to test itself, the program ROMs; the scratchpad RAM, the I/O chips, the Video Display Processors (VDPs) and the Video RAMs (VRAMs). If the uP finds all circuits in proper operating order it initializes the Vidiot Deluxe module and makes it ready for game play. If the uP finds a fault during the course of Self-Test, it stops at that point in the test and does not allow game play.

The accuracy of the Vidiot Deluxe Self-Test is about 90%. All faults except communications interface problems are detected.

The interesting idea behind the Vidiot Self-Test is that not only does it prevent operation when faults are detected, but like the MPU module, it helps to localize these faults. The LED indicator on the Vidiot Deluxe flashes once for each successfully completed test. Counting the number of flashes of the LED, after power-up, localizes the fault to the offending circuit of the module.

Both the Vidiot Deluxe and the Cheap-Squeak module use the same line for their LED's for Self-Test. The Cheap-Squeak module goes first while the Vidiot Deluxe waits for about 3 seconds. If the LED comes on after RESET and stays on, both the Cheap-Squeak and Vidiot Deluxe are not functioning properly. If the LED stays on or off for about 3 seconds, then starts flashing the Cheap-Squeak has a problem. If the LED flashes then stays on or off after about 3 seconds the Vidiot Deluxe has a problem.

A. 1st Flash

After RESET, the Cheap-Squeak (U1) attempts to test the sound ROM U3. It does a vertical sum of the ROM contents and checks for an all ones result. If the computed checksum is not all ones, U3 is defective and the uP will not allow sounds to be made. If the checksum is 11111111 the uP flashes the LED and proceeds to the next test.

B. 2nd Flash

Next the Cheap-Squeak (U1) tests its uP and the on-chip RAM. It attempts to write then read back all 256 patterns (00000000 to 11111111) in each of the 128 on-chip locations. If at any point in this test the uP fails to correctly read back a pattern it has written, U1 is deemed defective and the uP will not allow sounds to be made. If the uP completes the test successfully, it flashes the LED and awaits sound instructions from the Video section.
C. 3rd Flash

After a pause the Video uP (U2) attempts to test the program ROM U9. It performs a vertical sum of the ROM contents and checks this for an all ones result. If the computer checksum is not all ones, U9 is defective and the uP will not allow game play. If the checksum is 11111111, the uP flashes the LED and proceeds to the next test.

D. 4th Flash

Next the Video uP attempts to test ROM U8 in the same way. If the checksum is incorrect U8 is defective and the uP will not allow game play. If the checksum is correct, the uP flashes the LED and proceeds to the next test.

E. 5th Flash

This test is the same as the 4th flash but is performed on U7. A good ROM in U7 is indicated with a LED flash and the next test is started. A bad part in U7 will not allow game play.

F. 6th Flash

This test is the same as the 5th flash but is performed on U6. A good ROM in U6 is indicated with a LED flash and the next test is started. A bad part in U6 will not allow game play.

G. 7th Flash

This test is the same as the 6th flash but is performed on U5. A good ROM in U5 is indicated with a LED flash and the next test is started. A bad part in U5 will not allow game play.

H. 8th Flash

This test is the same as the 7th flash but is performed on U4. A good ROM in U4 is indicated with a LED flash and the next test is started. A bad part in U4 will not allow game play.

I. 9th Flash

Now the Video uP (U3) tests the scratch RAM U10. It attempts to write and read back an incrementing pattern that is not address aligned to all 2049 locations. It then attempts to write and read back a decrementing non-aligned pattern. If at any point in this test the uP fails to correctly verify the pattern it has written, U10 is deemed bad and the uP will not allow the Vidiot to come up. If the uP completes the test successfully, it flashes the LED and proceeds to the next test.

J. 10th Flash

The Video uP now tests the PIA chip U27. It tests each of the two full byte port initialization registers with a 256 pattern test (00000000 to 11111111). It tests each of the two full byte's I/O register, PA0-PA7 and PB0-PB7 with a 256 pattern test. It then tests the CA2 and CB2 ports. These are initialized as outputs then written into to see if they will store a '1' and a '0'. When both ports are found good, the uP flashes the LED and proceeds to the next test.
K. 11th Flash

The next test attempts to verify that the Master VDP (U18) is operating. The uP attempts to initialize the Master VDP registers for operation then monitors the "End of Frame" flag bit on one of the registers. After the first occurrence the up resets the bit and times its reoccurrence. The Master VDP should set this bit at the end of each video scan frame, about 60 Hertz. If this rate is not detected the up finds the Master VDP defective and won't allow the video to come up. If the rate is within tolerance the up flashes the LED and proceeds to the next test.

L. 12th Flash

This test attempts to verify that the Master VRAM (U19-U26) is operational. The uP tells the Master VDP the RAM type and size and allows it to start dynamic RAM refresh operation. It then attempts to write and read back an incrementing pattern that is not address aligned to all 16394 locations. If this succeeds the test is repeated with a decrementing pattern. When all tests are completed the up flashes the LED and proceeds to the next test.

M. 13th Flash

The next test attempts to verify that the Slave VDP (U28) is operating. The uP attempts to initialize the Slave VDP registers for operation then monitors the 'End of Frame' flag bit in one of the registers. After the first occurrence the uP resets the bit and times its reoccurrence. The Slave VDP should set this bit at the end of each video scan frame, about 60 Hertz. If this rate is not detected the uP finds the Slave VDP defective and won't allow the video to come up. If the rate is within tolerance the uP flashes the LED and proceeds to the next test.

N. 14th Flash

The last test attempts to verify the Slave VRAM (U29-U26). The uP tells the Slave VDP the RAM type and size and allows it to start dynamic RAM refresh operation. It then attempts to write and read back an incrementing pattern that is not address aligned to all 16384 locations. If this succeeds, the test is repeated with a decrementing pattern. When all tests are completed the up flashes the LED and proceeds to initialize the Vidiot for same play.

VIDIOT DELUXE INITIALIZATION

The Video uP initializes the PIA for MPU-Vidiot Deluxe communications, Video Joystick switch reading and Cheap-Squeak communications. It clears the scratch pad RAM and sets up the initial Video variables. It configures the VDPs and their VRAM parameter tables then awaits game play instructions from the MPU. No screen is displayed unless instructions are received from the MPU.

NORMAL OPERATION

The Vidiot Deluxe serves three functions. First, it is a display device for the MPU. Second it controls the Cheap-Squeak sound system for the MPU and itself. And lastly, it is a video game board.
The Vidiot Deluxe and MPU work together to provide an integrated Video Game with a Pinball feature. Their combined operation requires a coordinated inter-uP communication. This communication is provided by the interface on the Vidiot Deluxe module. Interface Data and Status is returned to the MPU on its switch return lines. The MPU controls this information flow by selectively enabling the Video Output or Status Data drivers synchronously with its switch reading. To send a byte of information to the MPU the video uP latches the data into U1 and sets a status bit that indicates that data is available. When the MPU polls the Vidiot Deluxe status data it detects the data available and subsequently reads the data by enabling U1 output drivers. The process of reading the data generates an interrupt to the video uP which causes it to clear the data available status bit. To send a byte of information to the Vidiot Deluxe the MPU latches the data into U2. The process of latching the data generates an interrupt to the video uP which causes it to set a status bit indicating the port is unavailable for writing. After the video uP reads the data byte it clears the status bit indicating more data may now be sent.

POWER SUPPLIES

The Vidiot Deluxe requires +12vdc & 4A unregulated voltage for its operation. All board voltages are derived from this source. The video uP, ROMs, RAMs and I/O and decode circuitry require +5vdc which is generated from this unregulated input by VR2, CR1, CR2, CR3, C131, C57, C58, C59, and C60. The Video Display Processors (VDPs) and their VRAMs also require +5vdc which is generated by VR3, CR4, CR5, CR6, C132, C61, C62, C63, and C64. The Video AMP Dematrix and Luma-Key circuitry require +8vdc which is generated by VR4, C69, C70, C71, C72. The Self-Test indicator requires +12vdc unregulated which is obtained from the +12vdc input to the module. This unregulated voltage is filtered for ESD protection before being used by any power supply by L1, C42, C43, C44, and C45.

RESET CIRCUIT

On power-up the uP requires +5vdc be applied for 100 milli-seconds before RESET is allowed to swing from 0 to 4.8v. The RESET circuit on the Vidiot Deluxe module works with the unregulated voltage to the regulator to prevent the RESET line from going high until the +5v supply has had time to stabilize after power-on. Zener diode VR1 and transistors Q2 and Q3 with R53 through R65 form a Valid Power Detector circuit that monitors the input voltage to VR2. This regulator requires a minimum of +7.5v input before it provides a +5v output. When this condition has been met diode CR7 allows C56 to charge through R69. This time constant provides the initial 100 MSEC delay to allow the uP oscillator to stabilize. The voltage across C56 is monitored by Q4, Q5, CR8, CR9 and R70 through R75. When it has reached about +2.5v the RESET line snaps high to allow the uP to start program execution. In the event that the input to VR2 drops below +7.5v for an instant Valid Power Detector quickly discharges C56 through R65 and CR7 to re-prime the RC time constant and insure a correct RESET cycle when power is re-applied.

This RESET signal is applied to the uP U3, the PIA U27, the VDPs U19 and U28.
VIDEO SECTION

The Vidiot Deluxe module video section is made up of three sub-sections. The uP, its address decoding, program RAM and program ROM form one section. The communication interface forms another sub-section, and the VDPs; VRAMs: Video AMP Dematrix and Luma-Key circuitry form the last sub-section.

A. Video uP, addressing decoding, program RAM and ROM

The Vidiot Deluxe module uses a high performance 8 bit micro-processor the MC68B09 as its video uP U3. This uP provides many 16 bit operations and a compact orthogonal instruction set with versatile addressing modes that maximizes the program performance. A bus cycle begins on the MC68B09 with the address and R/W lines changing to a known state. Shortly after they are stable the Q (quadrature) clock output goes high. One quarter of a bus cycle later the E (enable) clock output goes high. The addressed device on the bus places its data DO-D7 (R/W high) or takes its data from DO-D7 (R/W low) during the E clock. The bus cycle terminates when E goes low.

Addresses are decoded by U13, U14, U16, and U17 to determine which bus device the MC68B09 is accessing. The program ROMs U4 through U9 and RAM U10 are decoded with U14, a 3 to 8 line decoder. This decoder is enabled by the OR of Q and E via U13 to prevent spurious device selection during address line transitions. When address lines A13 through A15 are zero, decoder U14 enables a second decoder U16 to further decode this address space. This decoder provides the chip selects for the VDPs, the PIA and the communications interface, U1 and U2. Gate U17 re-establishes the timing of the VDP's chip selects to the E clock and allows the uP to write to both VDPs simultaneously at a certain address which improves program performance.

The program RAM is provided by U10. This is a 2K x 8 CMOS static RAM. The R/W line is combined with the OR of Q and E by U13 to provide a Write Enable signal and the R/W line is inverted by U15 to disable the RAM output drivers when the uP writes to the RAM. The program ROM is provided by U4 through U9. These sites accept 8K x 8 ROMs giving a maximum of 56K bytes of video program storage.

B. Communication Interface

The interface sub-section consists of U1, U2, U11, U12, U15 and U27. These parts work with the uP U3 to provide MPU-Vidiot Deluxe communication. Vidiot Deluxe switch reading and Vidiot Deluxe-Cheap Squeak communication. The MPU-Vidiot Deluxe communication was explained under NORMAL OPERATION above and will not be detailed here. The switch reading is performed by U27 which provides four switch strobes and eight switch returns that operates similar to the MPU switch read. The Vidiot Deluxe-Cheap Squeak communication uses the low order four switch returns of U27 and a strobe line, CB2. The information is passed as two half-bytes (nybbles) over these four lines, one per edge of the strobe line. The current timing for this process is below.

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\begin{align*}
\text{PBO-PB3} & \quad \text{1st Nybble LS} & \quad \text{2nd Nybble MS} \\
& \quad \langle -3 \text{ usec} \rangle & \quad \langle -3 \text{ usec} \rangle \\
\text{CB2} & \quad \langle -3 \text{ usec} \rangle & \quad \langle -15 \text{ usec} \rangle
\end{align*}
\]
The heart of the Vidiot Deluxe module is contained in the two VDPs. These LSI chips provide medium resolution video capability. The VDPs provide all necessary video, control and synchronization signals and also controls the storages, retrieval and refresh of data in the dynamic screen memory (VRAMs). They provide a 256 x 192 pixel pattern display in 15 colors with 32 object oriented patterns (sprites) that may be easily and smoothly moved with a minimum number of data operations. The uP U3 communicates with the VDPs over its data bus with three control lines. With this interface the uP can read or write to either VDP's VRAM, write either or both VDP control registers and read each VDP's status. The Master VDP interrupts the uP at the end of each raster scan to allow the uP to update the VRAMs during the blank screen vertical interval.

The Master and Slave VDPs are open-loop synchronized during RESET. Since they both use the same crystal for their oscillators; a simultaneous RESET with a fast enough risetime causes the internal timebases in both VDPs to start at the same time. Each VDP outputs color difference signals, Luminance (Y), Red minus Luminance (R-Y) and Blue minus Luminance (B-Y). The synchronizing information for the raster timing is contained in the Y outputs. The Y output of the Master VDP U18 is processed by part of U41 to provide the SYNC signal for the video monitor. The synchronization information is obtained by detecting the lowest levels of the Y signal. Half of U41, R148, R149, R162, RT4 and C121 form a comparator which compares the Y signal level against a reference provided by RT4 and R149. When the Y signal goes below the reference level the output of U41 goes high providing a positive going SYNC signal.

The three color difference signals from each VDP U18 and U29 go to the Luma-Key processing circuit. Each VDP's signals are buffered then offset corrected by U37, U38, U39, and associated components. Individual offset controls are provided to allow matching between VDPs. The buffered corrected signals are fed through switches, then combined in pairs and summed at the Video AMP Dematrix circuit. The switches for the Master VDP are R108, R113, R129, CR14, CR15, CR16, Q13, Q14, and Q15. The switches for the Slave VDP are R97, R93, R103, CR11, CR12, CR13, Q10, Q11, and Q12. Only the Master or Slave's switches are on a any time. The control for the switches is provided by a comparator formed by part of U40, R120 through R122 and RT3. This comparator monitors the Y (luminance) signal from the Slave VDP. During the raster scan whenever the Slave VDP has active picture information occurring the comparator output goes high and turns on the Master switches which prevents the Master VDP's video from reaching the Video AMP Dematrix. At the same time, U13 inverts the output from the Luma-Key comparator and turns off the Slave VDP's switches so now the Slave VDP's video is output. Thus, any non-black video signal from the Slave VDP is shown over any signal from the Master VDP which in effect overlays Slave video over Master video, switching between the two in real time.

The resulting keyed color difference signals have to be converted to red (R), green (G) and blue (B) signals for the color monitor. The Video AMP Dematrix does this and amplifies the signals to the levels required by the monitor.
Operational amplifiers U41 and U42 are high speed current mirror circuits. The Y and R-Y signals from the Master and Slave switches are summed at the plus input to U42 by R142 through R145 and amplified. These signals also contain a DC offset voltage that must be removed. Potentiometer R17 and R161 inject an adjustable current into the minus input of U42 which removes this offset and allows the red level to be adjusted. Likewise the Y and B-Y signals from the Master and Slave switches are summed in another section of U42 by R138 through R141 and amplified. Potentiometer RT6 and R153 act to remove the DC offset and allow blue level adjustment. The R-Y and B-Y signals have encoded in them a G-Y component. Resistors R123 through R126 sum this weighted component and present it to the minus input of U41 where it has the Y component added via R127 and R128. Potentiometer RT5 and R163 remove the DC offset and allow the green level to be adjusted.

The resulting R-G-B color signals and the SYNC information are filtered by a RLC circuit and output to the monitor.